We claim:

1. A method of processing data in a programmable processor, the method comprising:

decoding a single instruction for selectively arranging data, specifying a data selection operand and a first and a second register each having a register width, the first and second registers providing a plurality of data elements each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields each selecting one of the plurality of data elements; and

for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.

2. The method of claim 1 wherein each field of the data selection operand provides a sufficient number of bits to specify any one of the plurality of data elements.

3. The method of claim 2 wherein each field of the data selection operand has a width of n bits, wherein the plurality of data elements comprises 2^n data elements.

4. The method of claim 1 wherein the data selection operand is provided by a register specified by the single instruction .

5. The method of claim 4 wherein the data selection operand has a width equal to the specified register width.

6. The method of claim 1 wherein the catenated result is provided to a register.

7. The method of claim 1 wherein the plurality of data elements has a combined width equal to the width of the first register plus the width of the second register.

8. The method of claim 1 wherein the instruction further specifies a data element width of the plurality of data elements.

9. The method of claim 1 wherein each data element has a width of 8 bits.

10. The method of claim 1 wherein the catenated result has a width of 128 bits.

11. The method of claim 1 wherein for each field of the data selection operand, a relative location of the field within the data selection operand corresponds to a relative location of the predetermined position within the catenated result.

12. The method of claim 1 further comprising:

decoding a second single instruction specifying a third and a fourth register each containing a plurality of floating-point operands;

multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or products; and

providing the plurality of products to partitioned fields of a result register as a catenated result.

13. A method for selectively arranging data in a programmable processor, the method comprising:

decoding a single instruction specifying a data selection operand and a first register having a register width, the first register providing a plurality of data elements each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields each selecting one of the plurality of data elements; and

for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.

14. A computer-readable medium:

having instructions that instruct a computer system to perform operations,

at least some of the instructions including a group element selection instruction for selectively arranging data in a programmable processor, the group element selection instruction capable of instructing a computer to perform operations comprising:

decoding the group element selection instruction specifying a data selection operand and a first and a second register each having a register width, the first and second registers providing a plurality of data elements each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields each selecting one of the plurality of data elements; and

for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.

15. The computer-readable medium of claim 14 wherein each field of the data selection operand provides a sufficient number of bits to specify any one of the plurality of data elements.

16. The computer-readable medium of claim 15 wherein each field of the data selection operand has a width of n bits, wherein the plurality of data elements comprises 2^n data elements.

17. The computer-readable medium of claim 14 wherein the data selection operand is provided by a register specified by the single instruction .

18. The computer-readable medium of claim 17 wherein the data selection operand has a width equal to the specified register width.

19. The computer-readable medium of claim 14 wherein the catenated result is provided to a register.

20. The computer-readable medium of claim 14 wherein the plurality of data elements has a combined width equal to the width of the first register plus the width of the second register.

21. The computer-readable medium of claim 14 wherein the instruction further specifies a data element width of the plurality of data elements.

22. The computer-readable medium of claim 14 wherein each data element has a width of 8 bits.

23. The computer-readable medium of claim 14 wherein the catenated result has a width of 128 bits.

24. The computer-readable medium of claim 14 wherein for each field of the data selection operand, a relative location of the field within the data selection operand corresponds to a relative location of the predetermined position within the catenated result.

25. The computer-readable medium of claim 14 wherein at least some of the instructions further include a group floating point multiply instruction for multiplying floating point data in a programmable processor, the group floating point multiply instruction capable of instructing the computer to perform operations comprising:

decoding the group floating point multiply instruction specifying a third and a fourth register each containing a plurality of floating-point operands;

multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or products; and

providing the plurality of products to partitioned fields of a result register as a catenated result.

26. A computer-readable medium:

having instructions that instruct a computer system to perform operations,

at least some of the instructions including a group element selection instruction for selectively arranging data in a programmable processor, the group element selection instruction

capable of instructing a computer to perform operations comprising:

decoding the group element selection instruction specifying a data selection operand and a first register having a register width, the first register providing a plurality of data elements each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields each selecting one of the plurality of data elements; and

for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.

27. A computer data signal, embodied in a transmission medium:

having instructions that instruct a computer system to perform operations,

at least some of the instructions including a group element selection instruction for selectively arranging data in a programmable processor, the group element selection instruction capable of instructing a computer to perform operations comprising:

decoding the group element selection instruction specifying a data selection operand and a first and a second register each having a register width, the first and second registers providing a plurality of data elements each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields each selecting one of the plurality of data elements; and

for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.

28. The computer data signal of claim 27 wherein each field of the data selection operand provides a sufficient number of bits to specify any one of the plurality of data elements.

29. The computer data signal of claim 28 wherein each field of the data selection operand has a width of n bits, wherein the plurality of data elements comprises 2^n data elements.

30. The computer data signal of claim 27 wherein the data selection operand is provided by a register specified by the single instruction .

31. The computer data signal of claim 30 wherein the data selection operand has a width equal to the specified register width.

32. The computer data signal of claim 27 wherein the catenated result is provided to a register.

33. The computer data signal of claim 27 wherein the plurality of data elements has a combined width equal to the width of the first register plus the width of the second register.

34. The computer data signal of claim 27 wherein the instruction further specifies a data element width of the plurality of data elements.

35. The computer data signal of claim 27 wherein each data element has a width of 8 bits.

36. The computer data signal of claim 27 wherein the catenated result has a width of 128 bits.

37. The computer data signal of claim 27 wherein for each field of the data selection operand, a relative location of the field within the data selection operand corresponds to a relative location of the predetermined position within the catenated result.

38. The computer data signal of claim 27 wherein at least some of the instructions further include a group floating point multiply instruction for multiplying floating point data in a programmable processor, the group floating point multiply instruction capable of instructing the computer to perform operations comprising:

decoding the group floating point multiply instruction specifying a third and a fourth register each containing a plurality of floating-point operands;

multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or products; and

providing the plurality of products to partitioned fields of a result register as a catenated result.

39. A computer data signal, embodied in a transmission medium:

having instructions that instruct a computer system to perform operations,

at least some of the instructions including a group element selection instruction for selectively arranging data in a programmable processor, the group element selection instruction capable of instructing a computer to perform operations comprising:

decoding the group element selection instruction specifying a data selection operand and a first register having a register width, the first register providing a plurality of data elements each having an elemental width smaller than the register width, the data selection

operand comprising a plurality of fields each selecting one of the plurality of data elements; and

for each field of the data selection operand, providing the data element selected by the field to a predetermined position in a catenated result.

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